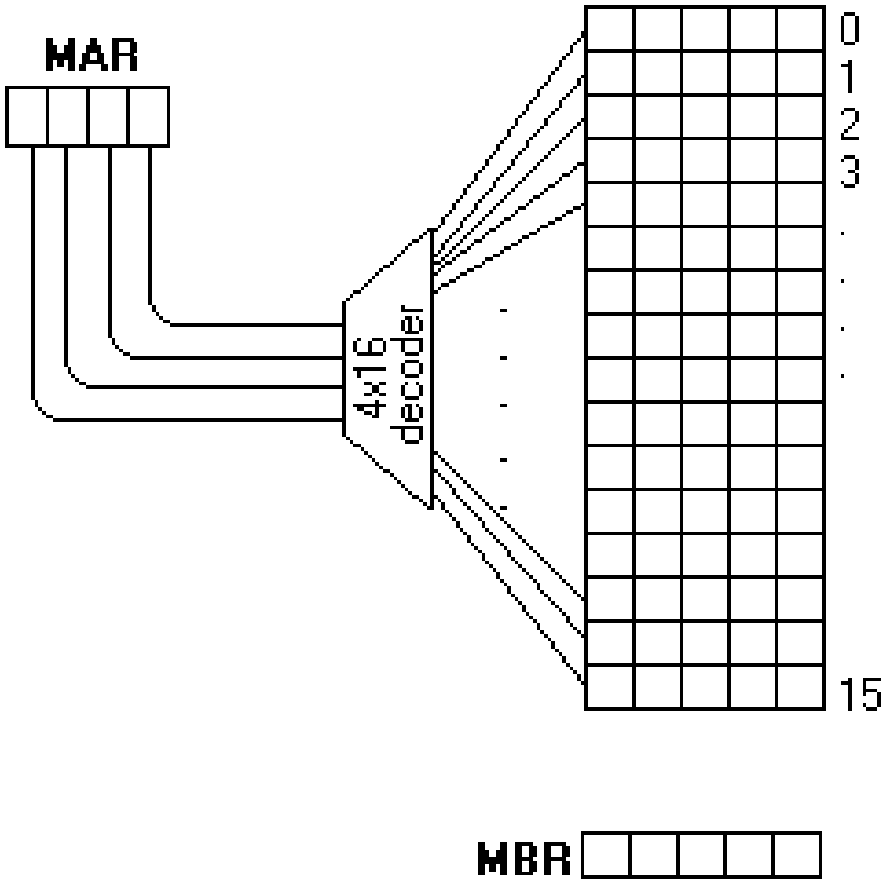
INTERNAL ORGANIZATION OF MEMORY CHIPS:

A memory consists of cells in the form of an array, in which each cell is capable of storing one bit of information. Each row of the cells constitutes a memory words and all cells of a row are connected to a common line referred to as a word line. Thus **W×b** memory has w words, each word having 'b' number of bits.

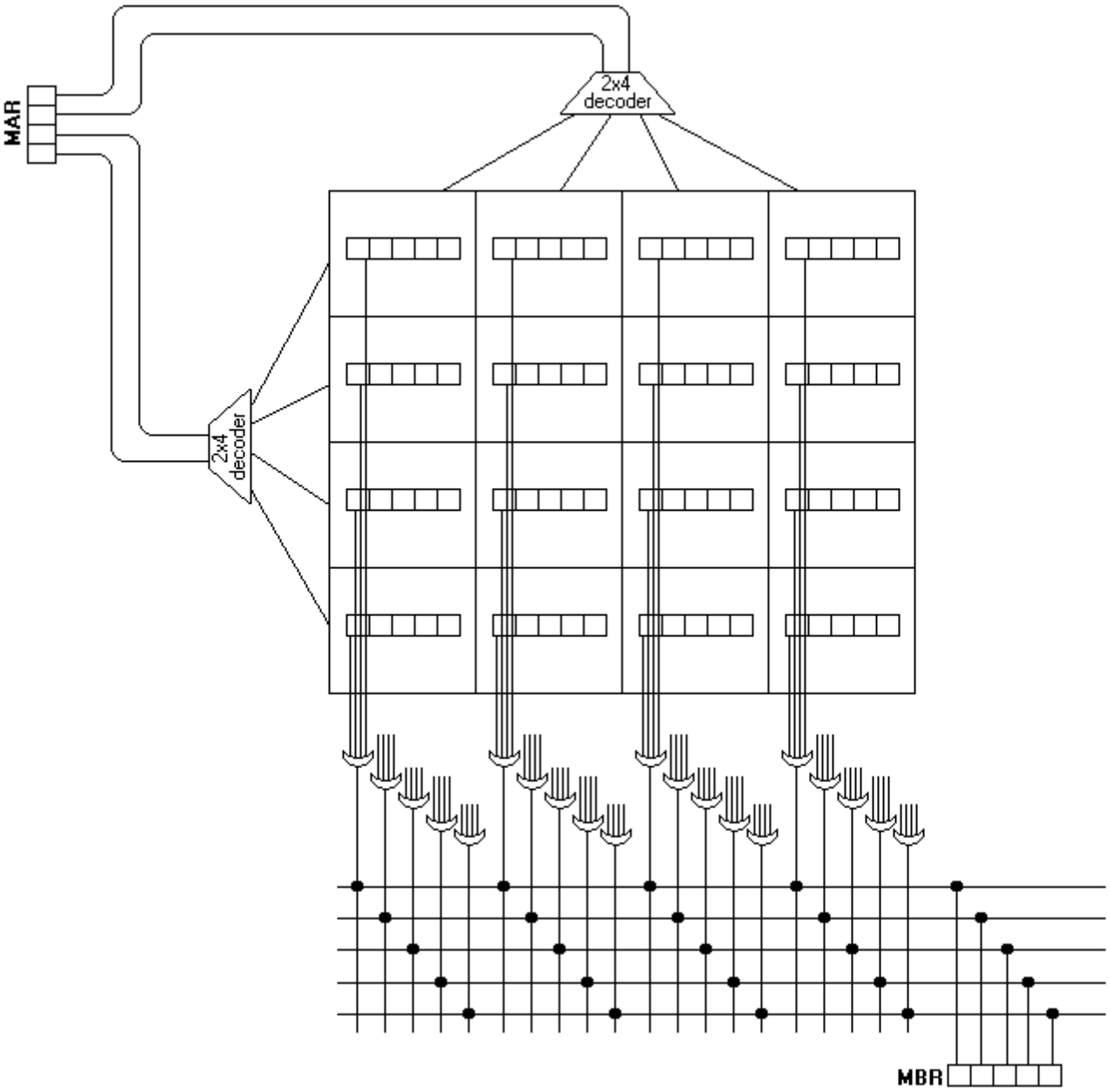
2D MEMORY ORGANIZATION: This is the simplest type of organization. The cells are organized in the form of a two dimensional array with rows and columns. Each row refers to a word line. The Memory address register (**MAR**) holds the address of the location where the read /write operation is executed. For a **W×b** memory, MAR has $\log_2 w=n$ bits. The content of MAR is decoded by an address decoder on the chip to activate each word line.

The **2D** memory organization for RAMs and ROMs mostly suffers from a problem of scale: it works fine when the number of words in the memory is relatively small but quickly mushrooms as the memory is scaled up or increased in size. This happens because the number of word select wires is an exponential function of the size of the address. As the number of address increases, number of selection wires also increases. This happens because the number of word select wires is an exponential function of the size of the address. Suppose that the MAR is 10 bits wide, which means there are 1024 words in the memory. The decoder will need to output 1024 separate lines. 1024 is not much larger but image 20 bits wide address; it will be 1024×1024 words.



Above figure shows a 16-word memory of 5-bit words using 2D Memory organization

2.5D MEMORY ORGANIZATION: One way to tackle the exponential explosion of growth in the decoder and word select wires is to organize memory cells into a two-dimension grid of words instead of a one-dimensional arrangement. Then the MAR is broken into two halves, which are fed separately into smaller decoders. One decoder addresses the rows of the grid while the other decoder addresses the columns.



Above figure shows a 16-word memory of 5-bit words using 2.5D Memory organization: Total number of word select lines goes down from 16 to 8.